SURFACE MOUNT LED

1.ELEMENT APPEARANCE

 DATE：2022.04.14

Model No.	Lighting Color	Resin Color
RT-IC2121RGB	Red	Water Clear
	Green	
	Blue	

2.ABSOLUTE MAXIMUM RATINGS AT Ta=25℃

Characteristic	Symbol		Rating	Unit
Forward direct current	I_{FM}	R	30	mA
		G	30	
		B	30	
Reverse voltage	V_{RM}		5	V
Operating temperature	Topr		-40 to +85	℃
Storage temperature	Tstg		-50 to +150	℃
Power dissipation	Pd	R	280	mW
		G	375	
		B	240	
Electrostatic Discharge	ESD		4K	V

3.ELECTRO-OPTICAL CHARACTERISTICS AT Ta=25℃

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Luminous intensity	Iv	IF=5mA	R	150	~	350	mcd
		IF=5mA	G	450	~	900	
		IF=5mA	B	70	~	250	
Forward voltage	V_F	IF=5mA	R	1.7	~	2.1	V
		IF=5mA	G	2.5	~	2.9	
		IF=5mA	B	2.6	~	3.2	
Reverse current	I_R	V_R=5V				5	μA
Dominant wavelength	λd	IF=5mA	R	615	~	630	nm
		IF=5mA	G	520	~	535	
		IF=5mA	B	460	~	475	
Viewing angle(X,Y)	2θ 1/2	IF=5mA			120		deg.

※Measurement Uncertainty of Luminous Intensity：±15%

※Measurement Uncertainty of Forward Voltage：±0.05V

※Peak emission wavelength Measurement allowance is ±1.0nm

Absolute Maximum Ratings (Ta=25℃,VSS=0V) ：

Symbol	Parameter	Range	Unit
Vin	DIN, FDIN port voltage	-0.4-VDD+0.5	V
Vout	OUT port voltage	-0.4-+5.5	V
Topr	Working temperature	-40-+85	℃
Tstg	Storage temperature	-50-+150	℃
VESD	ESD pressure	4000	V

Recommended working conditions(Test at -40～+85℃, unless otherwise specified)

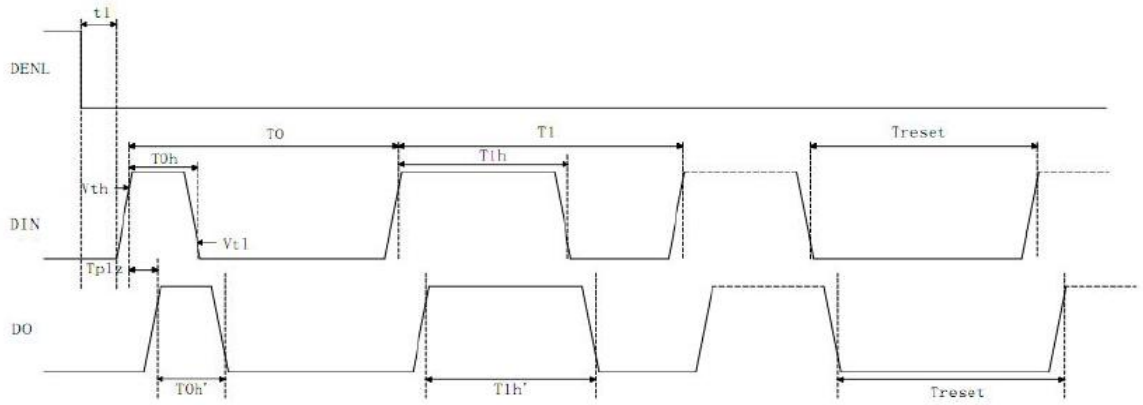
Symbol	Parameter	Range	Min	Typ	Max	Unit
VDD	voltage		3.5	-	5.5	V
Vin	DIN, FDIN port voltage	VDD=5V, DIN, FDIN series 1kΩ resistor	-	-	VDD+0.4	V
Vdo	D01, DO2 port voltage	VDD=5V, D01、D02 series 1kΩ resistor	-	-	VDD+0.4	V
Vout	OUT port voltage	OUT=OFF	-	-	5	V

Electrical specification (VDD=5V , Ta=25℃)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Voh	High level output voltage	Ioh=6mA	VDD-0.5	-	-	V
Vol	Low level output voltage	Iol=10mA	-	-	0.3	V
Vih	High level input voltage	VDD=5.0V	2.8	-	VDD	V
Vil	Low level input voltage	VDD=5.0V	0	-	1	V
Ioh	High level output current	VDD=5.0V,Vdo=4.9V	-	1.4	-	mA
Iol	Low level output current	VDD=5.0V,Vdo=0.4V	-	12	-	mA
Iin	Input Current	DIN, FDIN connected to VDD	-	500	-	μA
IDD	Quiescent Current	VDD=5.0V , IOUT "OFF"	-	1.3	-	mA
Iout	OUT output current	R,G,B=ON,Vout=3.0V	2	-	17	mA
Iolkg	OUT output leakage current	R,G,B=OFF,Vout=5.0V		-	0.3	μA
ΔIolc0	Constant current error between channels	R,G,B=ON,Vout=3.0V		-	±3	%
ΔIolc1	Constant current error between chips	R,G,B=ON,Vout=3.0V	-	-	±5	%

Dynamic parameter (VDD=5V , Ta=25℃)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Fin	Data rate			1.2		MHz
Fout	OUT PWM output	R,G,B		2		KHz
Tpz1	Transmission delay time	DIN→D01、D02 FDIN→D01、D02		150		ns
Ci	Input capacitance				15	pF



Name	Describe	Min	Typ	Max	Allowable error	Unit
T0h	Enter 0 code, high time	200	240	280	VDD=5.0V GND=0V	ns
T1h	Input 1 code, high time	400	480	560		ns
T0h'	Output 0 code, high time	200	240	280		ns
T1h'	Output 1 code, high time	400	480	560		ns
T0/T1	0 code or 1 code cycle		830			ns
Treset	Reset code, low time	80	-	-		ns

(1) The chip can work normally in the range of 830ns (frequency: 1.2mhz) to 2.5uS (frequency: 400KHz) with 0

Function description

Mode setting

This chip is single - line double - channel communication, using return - to - zero code to send signals. Before receiving display data, the chip needs to configure the correct working mode and select the mode of receiving display data. Mode setting commands are 48 bits, The first 24bit is the command code, and the last 24bit is the check inverse code. The chip starts to accept data after reset. The mode setting commands are as follows:

(1) 0XFFFFFF_000000

The chip is configured to work in normal mode. In this mode, DIN receives display data by default for the first time and the chip detects a message on the port Number input will keep the port received, if more than 160ms did not receive data, then switch to FDIN to receive data, chip detection If there is a signal input to this port, the port keeps receiving. If no data is received after 160ms, the port switches to DIN again Receive display data. DIN and FDIN are rotated in turn to receive display data.

(2) 0XFFFFFA_000005

The chip is configured to work in DIN mode. In this mode, the chip only receives the display data input from DIN terminal, and the FDIN terminal data is invalid.

(3) 0XFFFFF5_00000A command:

The chip is configured to work in FDIN mode. In this mode, the chip only receives the display data input from THE FDIN terminal, and the DATA input from the DIN terminal is invalid.

(4) 0XFFFFF0_00000F

The chip is configured in test mode

Display the data

After the chip is powered on and reset and receives mode setting commands, it starts to receive constant current setting commands, and then receives display data and receives 48bit After that, DO1 and DO2 ports begin to forward the continued data from DIN or FDIN to provide display data for the next cascaded chip. Forwarding data Previously, the DO1 and DO2 ports had been low. If DIN or FDIN input Reset signal, chip OUT port will receive according to The 48bit display data output corresponding duty cycle PWM waveform, and the chip is waiting to receive new data, after receiving the beginning of the 48bit After the data is received, the data is forwarded through the DO port. The original output of R, G, and B remains unchanged before the chip receives the Reset signal.

The chip adopts automatic shaping and forwarding technology to avoid distortion and attenuation of signal. For all cascaded chips, the data transfer period is Consistent.

A full frame data structure

C1	C2	C3	D1	D2	D3	D4	…	Dn	Reset	C1	C2	C3	D1	D2	D3	D4	…	Dn	Reset

C1 and C2 mode setting commands, each contains 24 bit data bits, each chip receives and forwarding C1 and C2, which is suitable for normal working mode 0 xffffff_000000 command, 0 xfffffa_000005 command for DIN work mode, 0 xfffff5_00000a work for FDIN mode command, 0 xfffff0_00000f command for the chip test mode, C3 is constant current value set command, every chip receives and forwarding C1, C2 and C3.

D1, D2, D3, D4... Dn is the PWM setting command for each chip.

Reset represents the Reset signal, and the low level is valid.

C3 data format

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

The C3 command contains 8×3bit data bits, the high order starts, and R7, G7, and B7 are fixed at 0.

R[6:0]: Used to set R output constant current value. All 0 code is 2mA, all 1 code is 25mA, 128 class adjustable.

G[6:0]: Used to set G output constant current value. All 0 code is 2mA, all 1 code is 25mA, 128 class adjustable.

B[6:0]: Used to set B output constant current value. All 0 code is 2mA, all 1 code is 25mA, 128 class adjustable.

The data format of Dn

R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

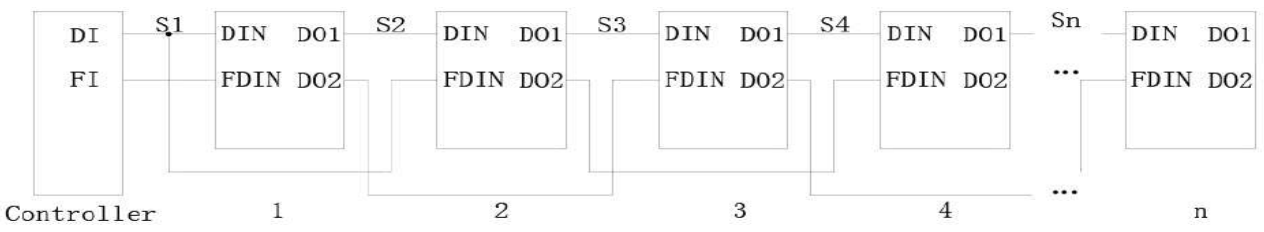
Each PWM setting command contains 8×3 bits of data, with the top starting

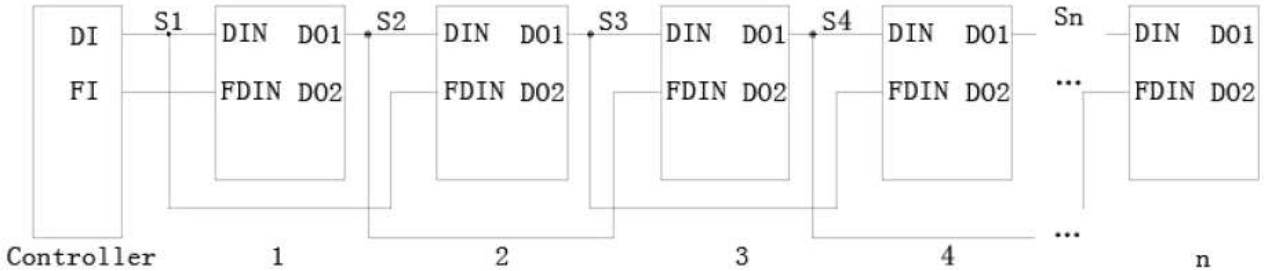
R[7:0]: Used to set the PWM duty ratio of R output. All 0 code is off, all 1 code is duty cycle maximum, 256 level adjustable

G[7:0]: Used to set the PWM duty ratio of G output. All 0 code is off, all 1 code is duty cycle maximum, 256 level adjustable

B[7:0]: Used to set the PWM duty ratio of B output. All 0 code is off, all 1 code is duty cycle maximum, 256 level adjustable.

data receiving and forwarding



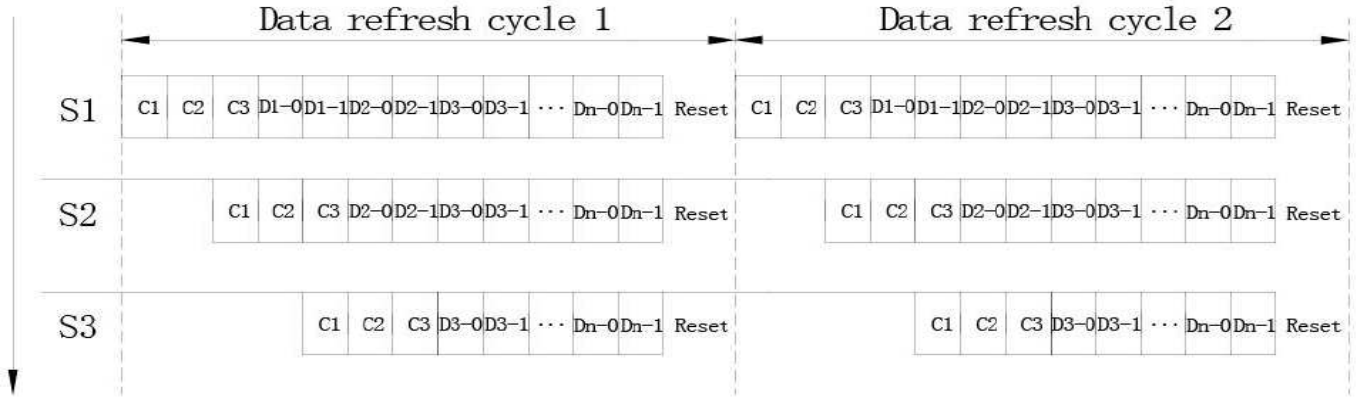


Where S1 is the data sent by controller Di port, S2, S3, S4 and Sn are the data forwarded by cascading TM1908.

Controller Di and Fi2 port data structure: C1C2C3D1D2D3D4... Dn.

Controller Fi port data structure: C1C2C3DxD1D2D3..... Dn.

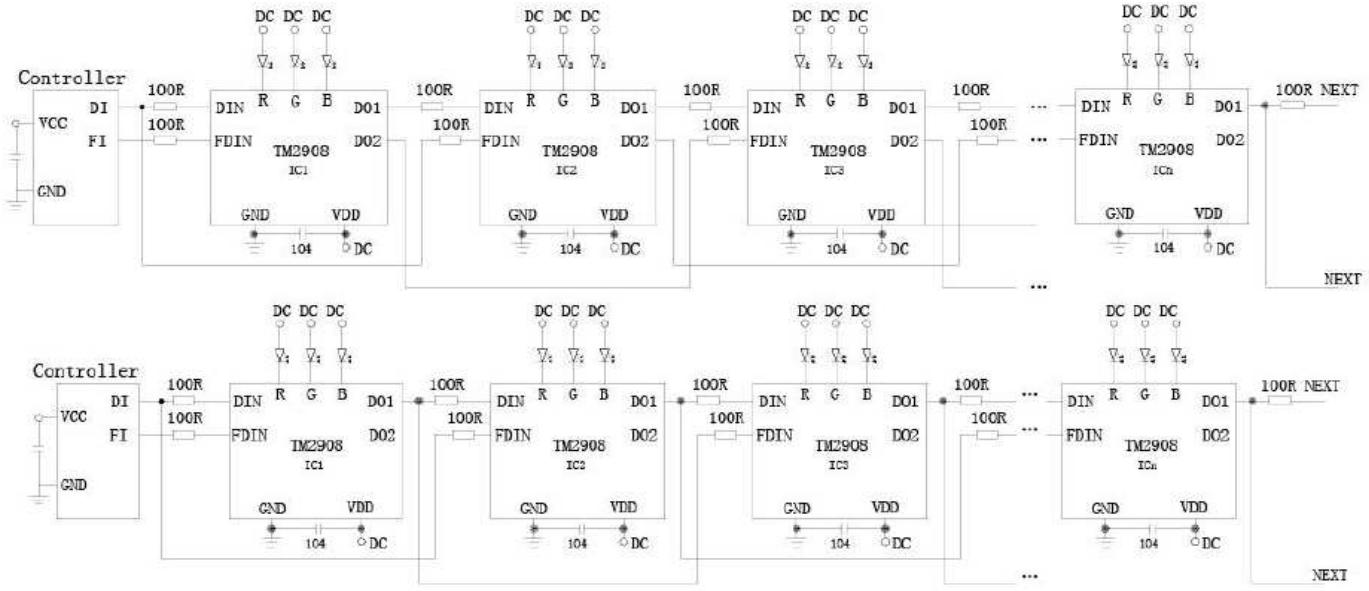
Where, Dx is any 24bit data bit.



The process of chip cascade and data transmission and forwarding is as follows: Controller sends data S1, chip 1 receives C1,C2 and C3 for verification. If the command is correct, it forwards C1,C2 and C3 and absorbs D1. If there is no Reset signal at this time, chip 1 will always forward the data sent by controller. Chip 2 also receives C1, C2 and C3 for verification. If the command is correct, it forwards C1, C2 and C3 and absorbs D2. If there is no Reset signal at this time, chip 2 will always forward the data sent by chip 1. And so on, until the controller sends a Reset signal, completes a data refresh cycle, and the chip is ready to receive again. Effective when Reset to low level. Maintain low level for longer than 80 s. Chip Reset.

Application information

Double cascade typical application circuit



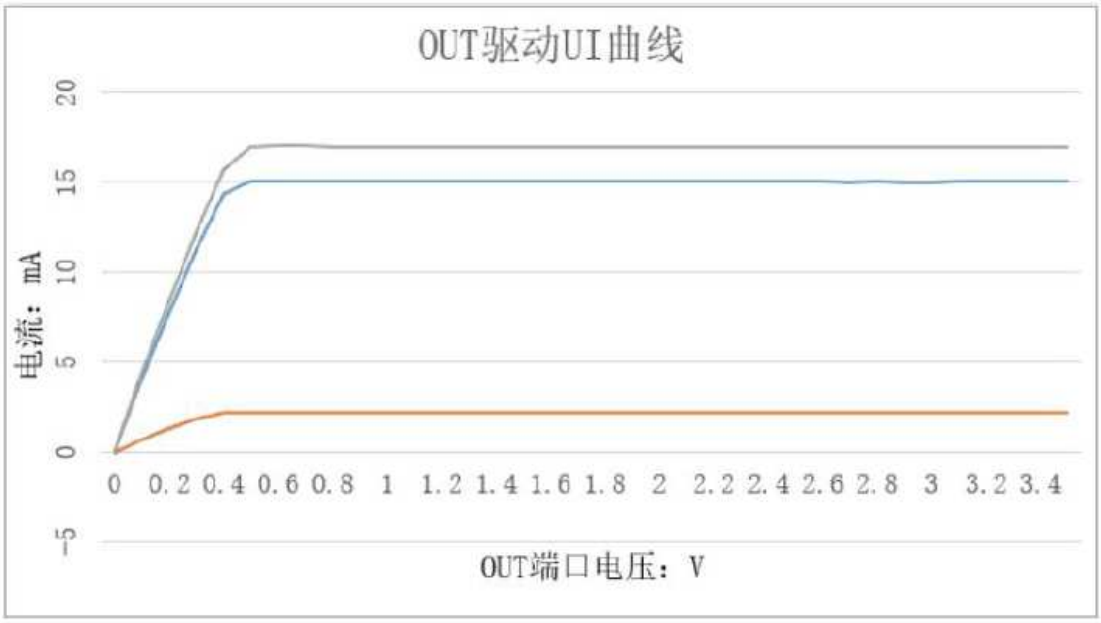
In order to prevent the chip signal input and output pins from being damaged due to the instantaneous high voltage generated when the product is plugged during testing, the signal input and output pins should be damaged during the test The output pin is connected to a 100 ω protection resistor in series. In addition, the 104 decoupling capacitor of each chip in the figure is indispensable and is routed to VDD and GND of the chip The foot should be as short as possible to achieve the best decoupling effect and stable chip operation.

How do I calculate the data refresh rate

The data refresh time is calculated based on how many pixels are connected in a system. A set of RGB is usually one pixel (or segment). A TM2908 chip can control a set of RGB.
Calculated in normal mode:
The 1-bit data period is 830ns (frequency: 1.2mhz), and the data of a pixel includes R (16bit), G (16bit), and B (16bit) 48bit, transmission time is 830ns×48≈40us. If a system has a total of 400 pixels, refresh all display time at once Is 40us×400=16ms (ignoring C1, C2 and Reset signal time), that is, refresh rate of one second is: 1÷16ms=62.5Hz. Below is the table of the highest data refresh rate corresponding to the number of cascaded points:

	Normal mode	
The pixel points	highest data refresh time（ms）	Maximum data refresh rate（Hz）
1~400	16	62.5

When TM2908 is applied to LED product design, the current difference between channels and even between chips is very small, when the load terminal voltage changes, the stability of its output current is not affected, and the constant current curve is shown as follows:

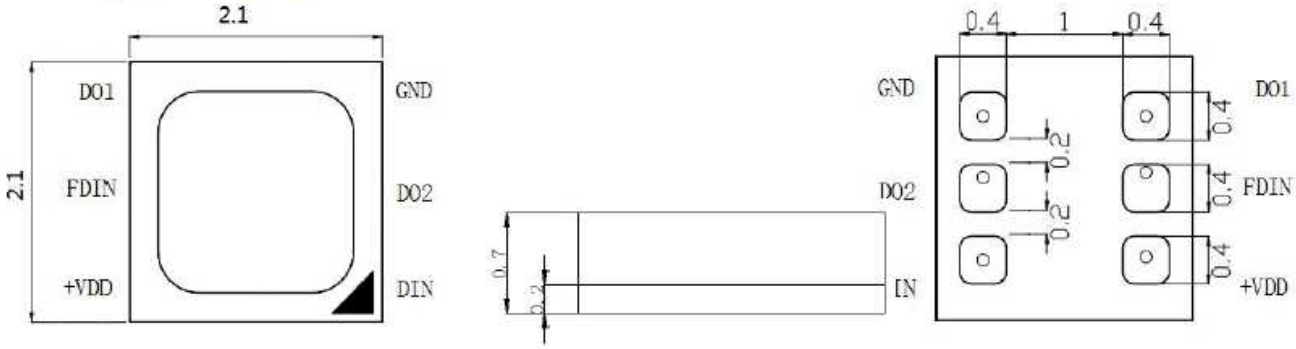


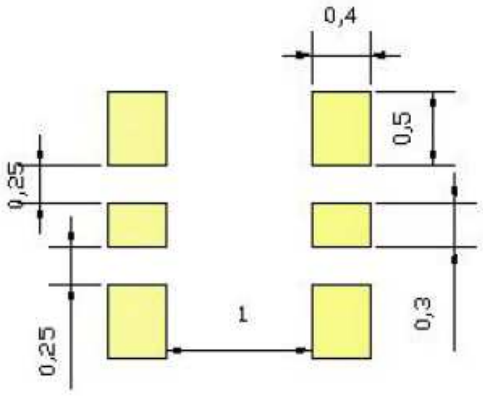
Coordinates

serial number	Foot a name	X(um)	Y（um）	PAD type	PAD size
1	G	58	470.38	binding PAD	80*80
2	R	58	343.38	binding PAD	80*80
3	vdd!	58	212.19	binding PAD	80*80
4	B	58	81	binding PAD	80*80
5	DIN	191.5	58	binding PAD	80*80
6	DO2	342	195	binding PAD	80*80
7	gnd!	342	322	binding PAD	80*80
8	DO1	314	497	binding PAD	80*80
9	FDIN	185	497	binding PAD	80*80

4.DIMENSIONS UNIT：m/m **TOLERANCE**：± 0.25m/m

Package Dimensions:



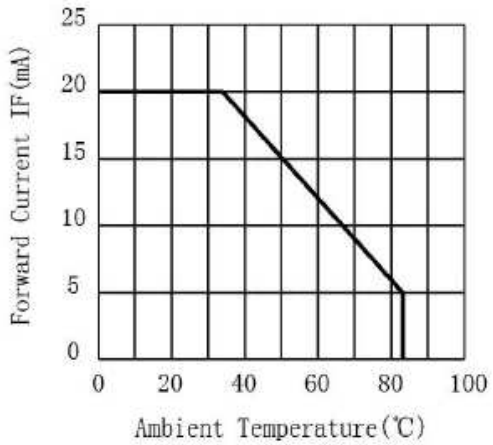


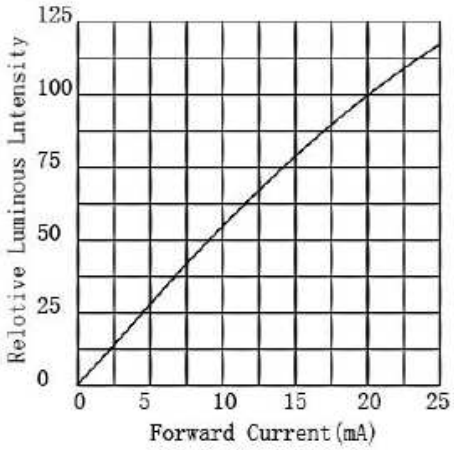
PIN function

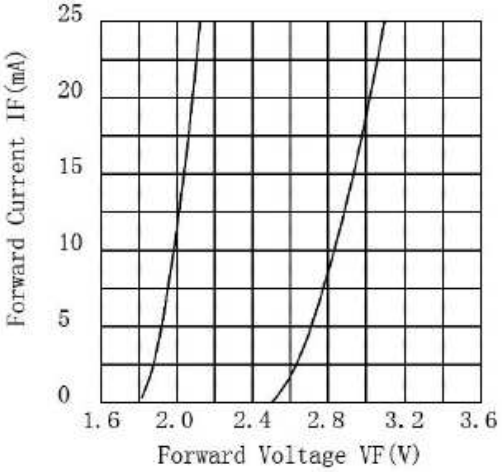
NO.	Symbol	Function description
1	FDIN	Alternate data input
2	VDD	Positive power supply
3	DIN	Signal input
4	DO1	Data cascading forwarding output 1
5	GND	Power ground
6	DO2	Data cascading forwarding output 2

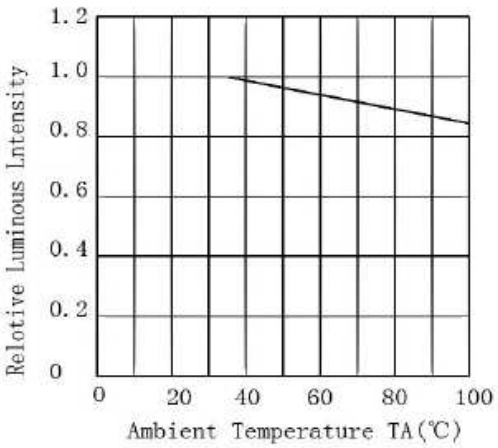
Typical optical characteristics curves

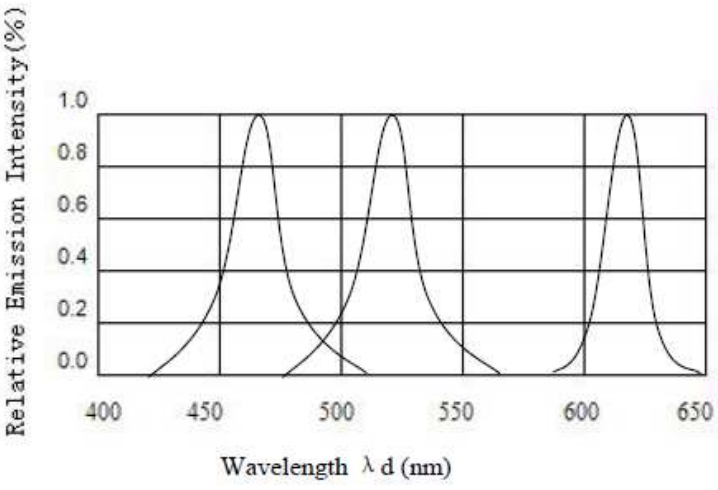
Ambient Temperature VS. Forward Current

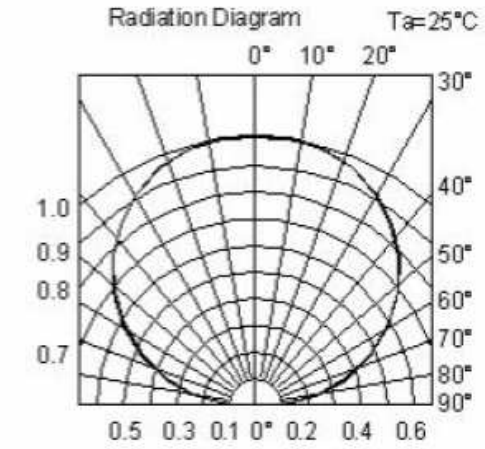








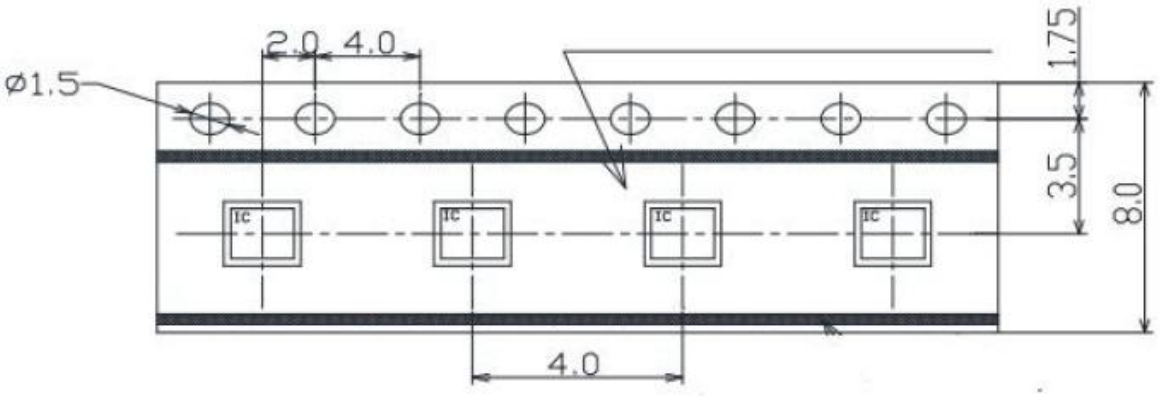




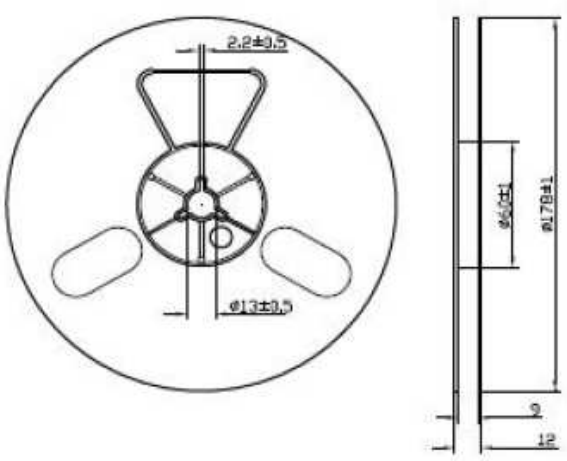
Model：RT-IC2121RGB

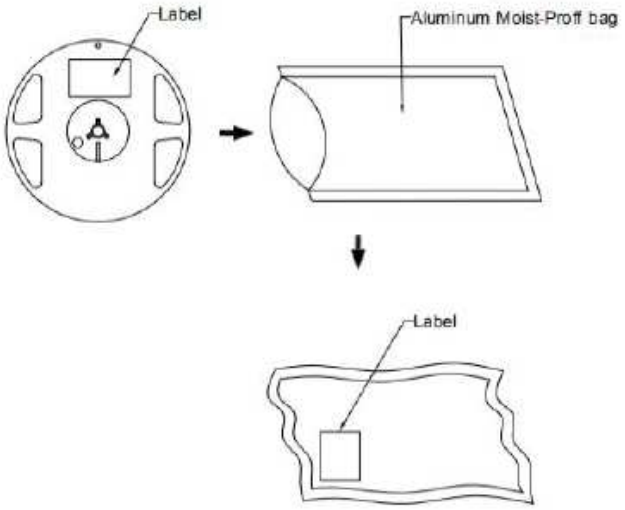
Tape Specifications (Units:mm)

Package: 4000pcs/reel



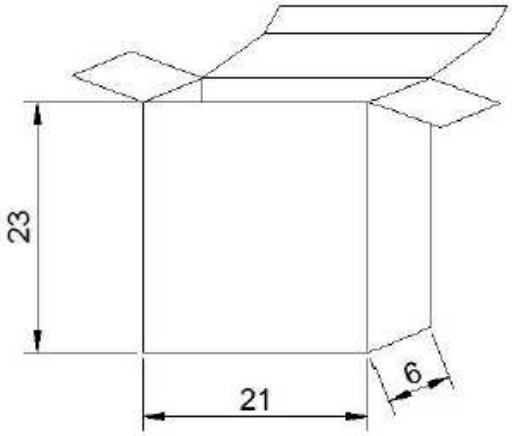
Moisture Resistant Packaging



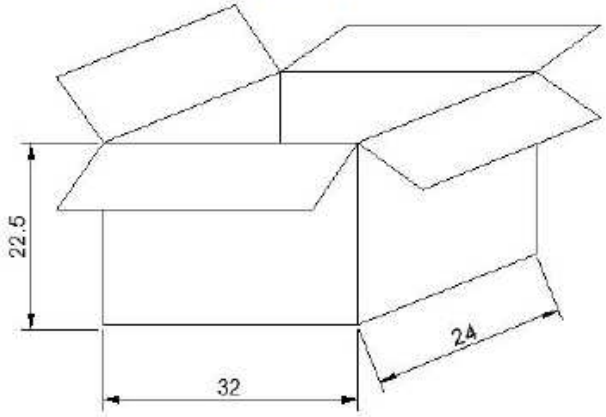


Cardboard Box

Maximum packing quantity (5 packs of material)



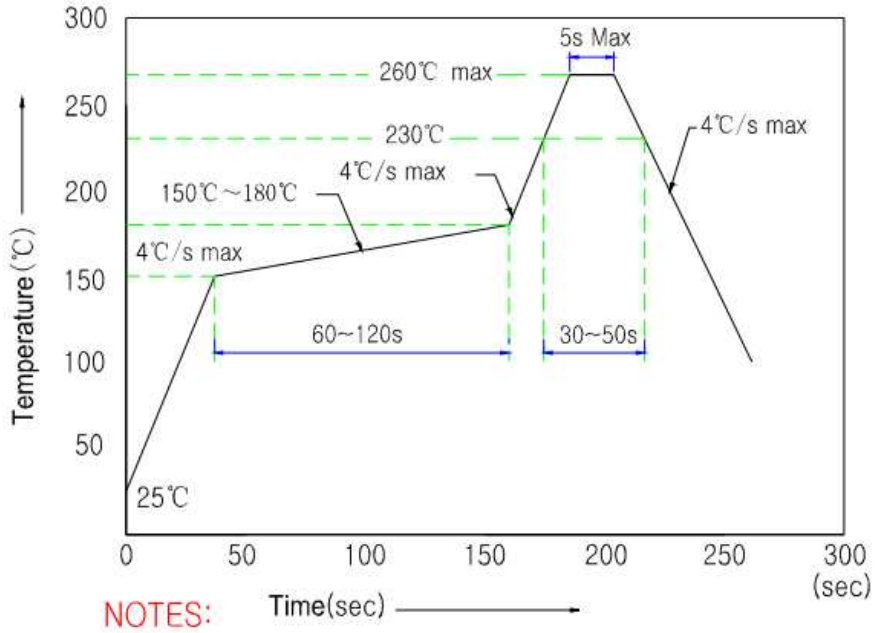
Maximum packing quantity (27 bags of material or 5 small boxes)



Reliability Test

Classification	Test Item	Test Conditions	Duration	Units Tested	Number of Damaged
Life Test	Operating Life Test	Ta =25℃±5℃, RH=55±20%RH, IF=30mA	1000hrs	22	0/22
Environment Test	High Temperature Storage	Ta =100℃±10℃	1000hrs	22	0/22
	Low Temperature Storage	Ta = - 40℃$^{+3}_{-5}$℃	1000hrs	22	0/22
	Temp &Humidity Storage	Ta =85℃$^{+5}_{-3}$ ℃ RH=85 $^{+5}_{-10}$ %RH	1000hrs	22	0/22
	Thermal Shock Test	Ta= - 40℃$^{+5}_{-3}$℃～ 100℃$^{+3}_{-5}$ ℃ T=5min - 5min	100 Cycles	22	0/22
	Temperature Cycling Test	Ta= - 40$^{+3}_{-5}$ ℃～25℃～ 100$^{+5}_{-3}$℃～25℃ T=30min-5min-30min-5min	10Cycles	22	0/22

Reflow Soldering Profile For Lead-free SMT Process.



NOTES:

1. We recommend the reflow temperature 245℃(+/-5℃). The maximum soldering temperature should be limited to 260℃.
2. Don't cause stress to the epoxy resin while it is exposed to high temperature.
3. Number of reflow process shall be 2 times or less.